PATENT ABSTRACTS OF JAPAN

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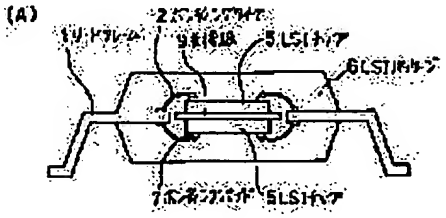
(71)Applicant : NEC CORP
NEC ENG LTD

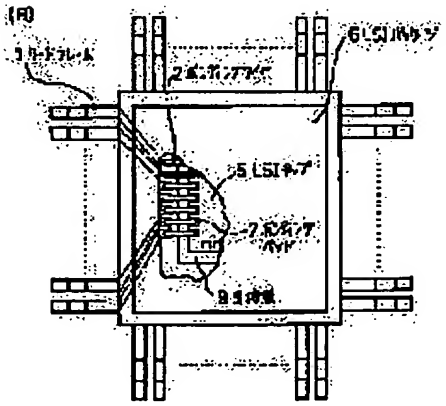
(72)Inventor : YOSHINO SUSUMU
CHIKAMA HIROKI

(54) INTEGRATED CIRCUIT DEVICE

(57)Abstract:



PURPOSE: To relax the limits to the integration density and to the number of signal pins of a single LSI chip when the LSI chip is mounted on an integrated circuit package and to relax the influence of a noise caused at the LSI chip and at leads.



CONSTITUTION: A plurality of LSI chips 5 are mounted at the upper part and the lower part so as to sandwich a support plate 9 or a support plate 9 which can be grounded. In such an integrated circuit structure, the LSI chips at the upper part and the lower part are connected to leads or a lead frame 1 by means of bonding wires 2. When the two chips at the upper part and the lower part are die-bonded, they are connected to the leads or the lead frame 1. The leads have a structure which is divided into the upper part and the lower part or into the right and the left so as to sandwich the support plate 9 which can be grounded; they are connected to the individual chips. Thereby, the chips can be integrated highly and mounted at high density, and their noise can be reduced.

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CLAIMS

[Claim(s)]
[Claim 1] The integrated circuit device characterized by mounting two or more LSI chips in the form which sandwiches a support plate.
[Claim 2] The integrated circuit device characterized by pasting up the rear faces or front faces of an LSI chip on the both sides of a support plate in the integrated circuit device shown in claim 1.
[Claim 3] The integrated circuit device with which the inner lead of an LSI chip is characterized by having the operation as a leadframe in the integrated circuit device shown in claim 1.
[Claim 4] The integrated circuit device characterized by enabling touch-down of a support plate in the integrated circuit device shown in claim 1.
[Claim 5] The integrated circuit device characterized by pulling out in a straight respectively in the integrated circuit device shown in claim 4 in the form which sandwiches a support plate from the LSI chip of the upper and lower sides of a lead.
[Claim 6] The integrated circuit device characterized by pulling out a bonding wire or a lead by turns from a vertical LSI chip as a lead in the integrated circuit device shown in claims 2 and 3.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to the mounting structure in the integrated circuit package of an LSI chip about an integrated circuit device.
[0002]
[Description of the Prior Art] As for the mounting technology to the conventional LSI package, the LSI chip was alone mounted in the support plate (die pad), the heat sink, etc. The leadframe and the LSI chip are connected by the bonding wire at this time. Moreover, there is a technique which carries out number chip mounting on a single side like a hybrid IC.
[0003]
[Problem(s) to be Solved by the Invention] In the conventional integrated circuit device mentioned above, since the LSI chip is mounted alone, a limitation is generated in a degree of integration or the number of signal pins. Moreover, since neither the external lead nor the LSI chip was grounded, it had the trouble of becoming easy to be influenced of a noise.
[0004]

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DETAILED DESCRIPTION

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[0003]
[Problem(s) to be Solved by the Invention] In the conventional integrated circuit device mentioned above, since the LSI chip is mounted alone, a limitation is generated in a degree of integration or the number of signal pins. Moreover, since neither the external lead nor the LSI chip was grounded, it had the trouble of becoming easy to be influenced of a noise.
[0004] Moreover, when a number chip is carried in a single side like a hybrid IC etc., a degree of integration needs the surface integral of the LSI chip mounted although it is large, and a led area around it, and has the problem that the whole area becomes large.
[0005]
[Means for Solving the Problem] The integrated circuit device of this invention is mounted up and down in the form which sandwiches a support plate or an earth plate for two or more LSI chips. And in this integrated-circuit structure, external RIDOHE connection is made by the bonding wire from a vertical LSI chip. Moreover, die bonding of the two chips is carried out up and down, the inner lead of both chips is fabricated as a lead, and it connects with an external lead. This lead is structure divided into the upper and lower sides or right and left on both sides of the support plate in which touch-down is possible, and is connected to each chip. Or there is also structure which pulls out an inner lead as a lead by turns from vertical 2 chip.
[0006]
[Function] Since the integrated circuit device of this invention is constituted by the above structures, both the area and volume to occupy are reduced, and whenever [electric electric shielding-with the exterior] increases, and its electric noise jamming from the outside decreases, and it can have a good operating characteristic.
[0007]
[Example] Next, this invention is explained with reference to a drawing.
[0008] drawing 1 -- the example of claims 1 and 2 of this invention, and drawing 2 R> -- in 2 and 3, the example of claims 1, 2, 3, and 5 and drawing 4 show the example of claims 1, 2, and 3, and drawing 5 shows the example of claims 1, 2, 3, and 4, respectively.
[0009] Drawing 1 (A) is drawing of longitudinal section of one example of this invention, and drawing 1 (B) is a plan. the support plate 9 in the LSI package 6 -- die bonding of LSI chip 5 is carried out up and

down, and the bonding wire 2 connects with the leadframe 1 by turns from the bonding pad 7 of the LSI chip of each upper and lower sides.

[0010] drawing 2 (A) -- a part of longitudinal section of other one example of this invention -- a Fig. and drawing 2 (B) -- a part of the top face -- it is a Fig. As inner lead A3 and inner lead B4 which are connected with the bonding pad 7 of LSI chip 5 sandwich the lead support plate 19, they paste up, and they are formed as a lead. Inner lead A3 of the lead support plate 19 and the upper and lower sides and B4 are pasted up through the insulating film 8. Inner leads A and B show the lead which the LSI chip of a support plate 9 top and the bottom connects, respectively here.

[0011] Drawing 2 (A) and (B) are pasted up through the support plate 9 for touch-down so that the front faces of an LSI chip may face each other, and the front face of LSI is protected by rubber 10.

[0012] Next, drawing 3 (C) and (D) are other drawings of longitudinal section and top views of one example of this invention, respectively. Drawing 3 (C) and (D) are one example at the time of drawing 2 (A) and (B) receiving up and down, and pasting up lead (inner lead A) 3 and lead (inner lead B) 4 on a both-sides side on both sides of a support plate 9.

[0013] drawing 4 (A) and (B) -- a part of longitudinal section of other one example of this invention -- a part of Fig. and its top face -- it is a Fig. And as inner lead A3 and inner lead B4 also sandwich a support plate 9, they paste up, and drawing 4 (A) and (B) form a lead for them at the same time they paste up the rear faces of LSI chip 5 through a support plate 9. [as well as drawing 2 and 3]

[0014] drawing 5 (A) and (B) -- a part of longitudinal section of other one example of this invention -- a part of Fig. and its top face -- it is a Fig. moreover, drawing 5 (C) and (D) -- a part of longitudinal section of other one example of this invention -- a part of Fig. and its top face -- it is a Fig. And drawing 5 (A) and (B) are examples when the rear faces of an LSI chip, drawing 5 (C), and (D) paste up the front faces of an LSI chip on a support plate 9.

[0015] And drawing 5 (A), (B), (C), and (D) show the configuration when pulling out by turns the leads (inner leads A and B) 3 and 4 which come out of the bonding pad 7 of the LIS chip 5 as a lead from LSI chip 5 of the upper bottom.

[0016] Moreover, drawing 5 (E) is the expansion partial diagrammatic view of drawing 5 (C). This drawing has shown as one example for grounding. There is lead 3 (inner lead A) connected to LSI chip 5 through the bonding pad 7, and the support plate is connected with the bonding pad 7 through the pad 11 for touch-down in the opposite side. A support plate will also be grounded if this lead is grounded.

[0017]

[Effect of the Invention] As explained above, it became possible to raise the degree of integration conventional by mounting an LSI chip so that a support plate may be inserted of this invention by leaps and bounds.

[0018] Moreover, reduction of a noise can be aimed at by mounting so that a support plate may be grounded and a support plate may be inserted by whenever [LSI chip or external Lee], and since the external lead for two chips can be done in one by inserting a support plate (earth plate), it is effective in the ability to perform high-density mounting.

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TECHNICAL FIELD

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PRIOR ART

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EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, it became possible to raise the degree of integration conventional by mounting an LSI chip so that a support plate may be inserted of this invention by leaps and bounds.
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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In the conventional integrated circuit device mentioned above, since the LSI chip is mounted alone, a limitation is generated in a degree of integration or the number of signal pins. Moreover, since neither the external lead nor the LSI chip was grounded, it had the trouble of becoming easy to be influenced of a noise.
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MEANS

[Means for Solving the Problem] The integrated circuit device of this invention is mounted up and down in the form which sandwiches a support plate or an earth plate for two or more LSI chips. And in this integrated-circuit structure, external RIDOHE connection is made by the bonding wire from a vertical LSI chip. Moreover, die bonding of the two chips is carried out up and down, the inner lead of both chips is fabricated as a lead, and it connects with an external lead. This lead is structure divided into the upper and lower sides or right and left on both sides of the support plate in which touch-down is possible, and is connected to each chip. Or there is also structure which pulls out an inner lead as a lead by turns from vertical 2 chip.

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OPERATION

[Function] Since the integrated circuit device of this invention is constituted by the above structures, both the area and volume to occupy are reduced, and whenever [electric electric shielding-with the exterior] increases, and its electric noise jamming from the outside decreases, and it can have a good operating characteristic.

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EXAMPLE

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[0010]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing of longitudinal section (A) and the plan (B) of one example of this invention.
[Drawing 2] It is partial drawing of longitudinal section (A) and the partial plan (B) of one example of this invention.
[Drawing 3] It is drawing of longitudinal section (C) and the plan (D) of one example of this invention.
[Drawing 4] It is partial drawing of longitudinal section (A) and the partial plan (B) of one example of this invention.
[Drawing 5] It is partial drawing of longitudinal section (A) of one example of this invention, a partial plan (B), and partial drawing of longitudinal section (C) and the partial plan (D) of other one example, and (E) is the enlarged drawing of partial drawing of longitudinal section of (C).
[Description of Notations]
1 Leadframe
2 Bonding Wire
3 Lead (Inner Lead A)
4 Lead (Inner Lead B)
5 LSI Chip
6 LSI Package
7 Bonding Pad
8 Insulating Film
9 Support Plate
10 Rubber
11 Pad for Touch-down
19 Lead Support Plate

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（A）　(11)特許出願公開番号

特開平5－136323

(43)公開日　平成５年(1993)６月１日

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		Ｎ　9272－4M		

審査請求　未請求　請求項の数６(全　６　頁)

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(71)出願人　000004237
日本電気株式会社
東京都港区芝五丁目７番１号

(71)出願人　000232047
日本電気エンジニアリング株式会社
東京都港区西新橋３丁目20番４号

(72)発明者　吉野　進
東京都港区芝五丁目７番１号　日本電気株式会社内

(72)発明者　千釜　広樹
東京都港区西新橋三丁目20番４号　日本電気エンジニアリング株式会社内

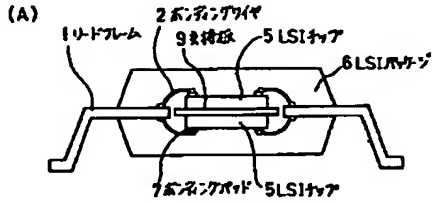
(74)代理人　弁理士　若林　忠

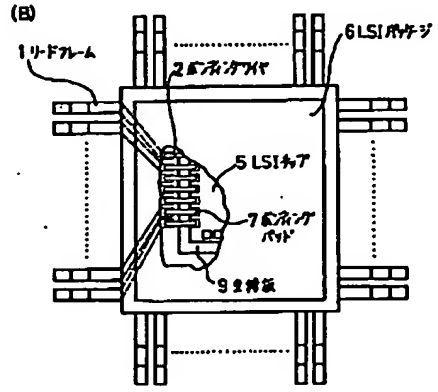
(54)【発明の名称】　集積回路装置

(57)【要約】

【目的】　集積回路パッケージにＬＳＩチップを実装する場合にＬＳＩチップ単体では、集積度や信号ピン数に限界がある。また、ＬＳＩチップやリードはノイズの影響を受け易いため、これらを緩和することを目的とする。

【構成】　複数のＬＳＩチップ５は支持板９または、接地可能な支持板を挟む形で上下に実装されている。そしてこの集積回路構造において、上下ＬＳＩチップからボンディングワイヤ２によりリードまたはリードフレーム１へ接続する。また上下の２チップをダイボンディングすることによりリードまたはリードフレーム１と接続する。このリードは、接地可能な支持板９を挟んで上下または左右に分割される構造であり、各々のチップに接続されている。これにより、高集積で高密度な実装が可能となり、かつノイズの低減を図れるようになった。





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【特許請求の範囲】

【請求項１】　複数のＬＳＩチップを支持板を挟む形で実装することを特徴とする集積回路装置。

【請求項２】　請求項１に示した集積回路装置において、支持板の両側にＬＳＩチップの裏面同士または表面同士を接着したことを特徴とする集積回路装置。

【請求項３】　請求項１に示した集積回路装置において、ＬＳＩチップのインナーリードが、リードフレームとしての作用を有することを特徴とする集積回路装置。

【請求項４】　請求項１に示した集積回路装置において、支持板を接地可能とすることを特徴とする集積回路装置。

【請求項５】　請求項４に示した集積回路装置において、リードを上下のＬＳＩチップから支持板を挟む形で各々ストレートに引き出すことを特徴とする集積回路装置。

【請求項６】　請求項２，３に示した集積回路装置において、リードとして上下ＬＳＩチップからボンディングワイヤまたは、リードを交互に引き出したことを特徴とする集積回路装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、集積回路装置に関し、特にＬＳＩチップの集積回路パッケージにおける実装構造に関する。

【０００２】

【従来の技術】従来のＬＳＩパッケージへの実装技術は、ＬＳＩチップが支持板（ダイ・パッド）や放熱板等に単体で実装されていた。この時、リードフレームとＬＳＩチップは、ボンディングワイヤにより接続されている。また、ハイブリッドＩＣのように単一面上で数チップ実装する技術がある。

【０００３】

【発明が解決しようとする課題】上述した従来の集積回路装置では、ＬＳＩチップが単体で実装されているため、集積度や信号ピン数に限界が生ずる。また、外部リードやＬＳＩチップは、接地されていないため、ノイズの影響を受け易くなるという問題点があった。

【０００４】また、ハイブリッドＩＣ等のごとく単一面に数チップが搭載される場合は、集積度は大きいが実装するＬＳＩチップの面積分とその周りのリード分の面積を必要とし全体の面積が大きくなるという問題がある。

【０００５】

【課題を解決するための手段】本発明の集積回路装置は、複数のＬＳＩチップを支持板または、接地板を挟む形で上下に実装している。そして、この集積回路構造において上下ＬＳＩチップからボンディングワイヤにより外部リードへ接続する。また、上下に２チップをダイボンディングし、両チップのインナーリードをリードとして成形し外部リードと接続する。このリードは、接地可

2

能な支持板を挟んで上下または左右に分割される構造であり、各々のチップに接続されている。或いは、上下２チップから交互にインナーリードをリードとして引き出す構造もある。

【０００６】

【作用】本発明の集積回路装置は上記のような構造に構成されるので、占有する面積と体積が共に縮小され、また外部との電気的遮蔽度が増大し、外部からの電気的雑音妨害が少なくなり、良好な動作特性を持つことができる。

【０００７】

【実施例】次に本発明について図面を参照して説明する。

【０００８】図１は本発明の請求項１，２の実施例、図２，３は請求項１，２，３，５の実施例、図４は請求項１，２，３の実施例、図５は請求項１，２，３，４の実施例をそれぞれ示している。

【０００９】図１（Ａ）は、本発明の一実施例の縦断面図であり、図１（Ｂ）は、上面図である。ＬＳＩパッケージ６内の支持板９の上下にＬＳＩチップ５がダイボンディングされており、上下各々のＬＳＩチップのボンディングパッド７から交互にボンディングワイヤ２によりリードフレーム１に接続されている。

【００１０】図２（Ａ）は、本発明の他の一実施例の縦断面の一部分図、図２（Ｂ）は、その上面の一部分図である。ＬＳＩチップ５のボンディングパッド７と接続されているインナーリードＡ３、インナーリードＢ４がリード支持板１９を挟むようにして接着され、リードとして形成されている。リード支持板１９と上下のインナーリードＡ３，Ｂ４は、絶縁フィルム８を介して接着されている。ここにインナーリードＡとＢとはそれぞれ支持板９の上と下のＬＳＩチップの接続するリードを示す。

【００１１】図２（Ａ），（Ｂ）は、ＬＳＩチップの表面同士が向き合うように接地用の支持板９を介して接着し、ＬＳＩの表面はラバー１０により保護されている。

【００１２】次に図３（Ｃ），（Ｄ）はそれぞれ本発明の他の一実施例の縦断面図と平面図である。図３（Ｃ），（Ｄ）は、リード（インナーリードＡ）３、リード（インナーリードＢ）４を図２（Ａ），（Ｂ）の上下に対し、支持板９を挟んで両側面に接着した場合の一実施例である。

【００１３】図４（Ａ），（Ｂ）は本発明の他の一実施例の縦断面の一部分図とその上面の一部分図である。そして図４（Ａ），（Ｂ）は、ＬＳＩチップ５の裏面同士を支持板９を介して接着すると同時に、図２，３と同様にインナーリードＡ３、インナーリードＢ４も支持板９を挟むようにして接着し、リードを形成する。

【００１４】図５（Ａ），（Ｂ）は本発明の他の一実施例の縦断面の一部分図とその上面の一部分図である。また図５（Ｃ），（Ｄ）も本発明の他の一実施例の縦断面

3

の一部分図とその上面の一部分図である。そして図5（A），（B）はＬＳＩチップの裏面同士、図5（C），（D）はＬＳＩチップの表面同士を支持板9に接着した場合の実施例である。

【００１5】そして図5（A），（B），（C），（D）はＬＩＳチップ5のボンディングパッド7から出るリード（インナーリードA，B）3，4を上、下のＬＳＩチップ5から交互にリードとして引き出したときの構成を示す。

【００１６】また、図5（E）は、図5（C）の拡大部分図である。この図では、接地するための一実施例として示してある。ボンディングパッド7を介してＬＳＩチップ5に接続されているリード3（インナーリードA）があり、ボンディングパッド7と反対側に接地用パッド１１を介して支持板が接続されている。このリードを接地すれば支持板も接地されることになる。

【００１７】

【発明の効果】以上説明したように本発明は、支持板を挟むようにＬＳＩチップを実装することで従来の集積度を飛躍的に向上させることが可能となった。

【００１８】また、支持板を接地してＬＳＩチップや外部リー度で支持板を挟むように実装することで、ノイズの低減を図ることができ、2チップ分の外部リードを支持板（接地板）を挟むことで1本にできるため、高密度な実装ができるという効果がある。

【図面の簡単な説明】

4

【図１】本発明の一実施例の縦断面図（A）と上面図（B）である。

【図２】本発明の一実施例の部分縦断面図（A）と部分上面図（B）である。

【図３】本発明の一実施例の縦断面図（C）と上面図（D）である。

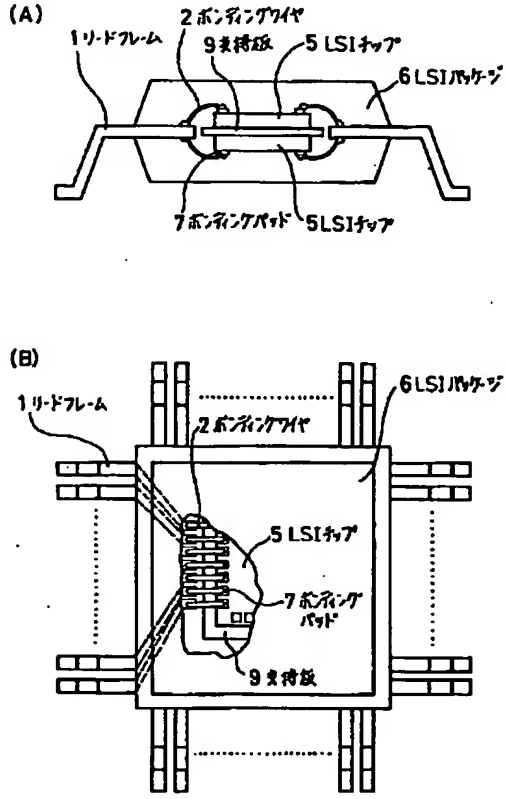
【図４】本発明の一実施例の部分縦断面図（A）と部分上面図（B）である。

【図５】本発明の一実施例の部分縦断面図（A）と部分上面図（B）及び他の一実施例の部分縦断面図（C）と部分上面図（D）であり、また（E）は（C）の部分縦断面図の拡大図である。

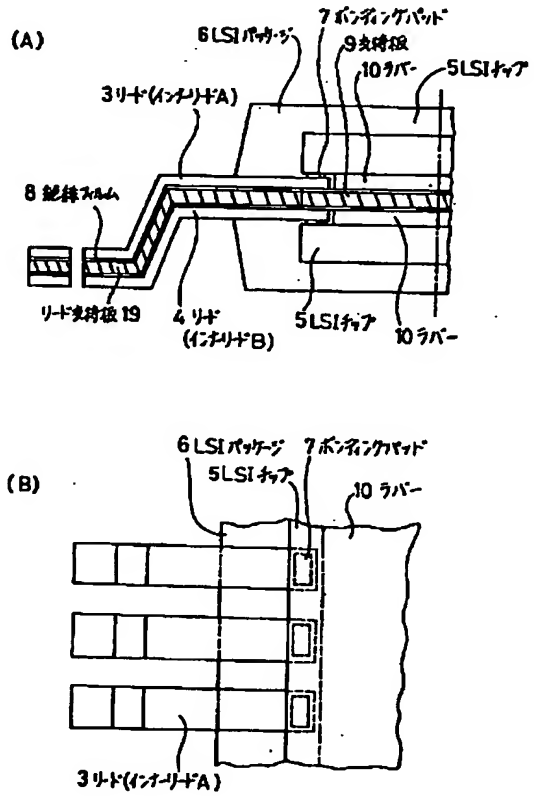
【符号の説明】

1　リードフレーム
2　ボンディングワイヤ
3　リード（インナーリードA）
4　リード（インナーリードB）
5　ＬＳＩチップ
6　ＬＳＩパッケージ
7　ボンディングパッド
8　絶縁フィルム
9　支持板
１０　ラバー
１１　接地用パッド
１９　リード支持板

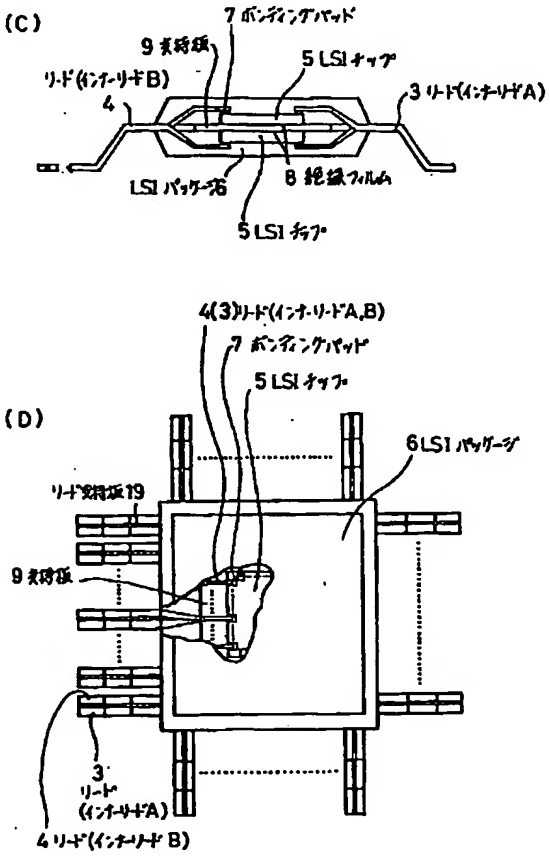
【図1】


(A)
1リードフレーム
2ボンディングワイヤ
9支持板
5 LSIチップ
6 LSIパッケージ
7ボンディングパッド
5LSIチップ
(B)
1リードフレーム
2ボンディングワイヤ
6 LSIパッケージ
5 LSIチップ
7ボンディングパッド
9支持板

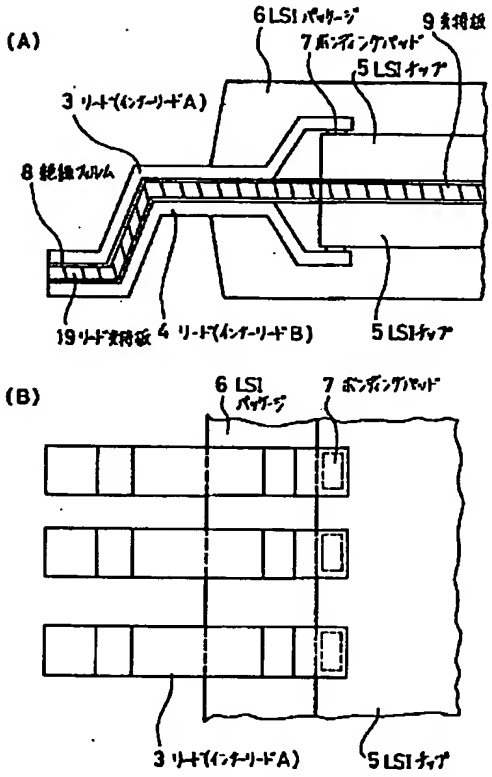
【図2】


(A)
6LSIパッケージ
7ボンディングパッド
9支持板
10ラバー
5LSIチップ
3リード(インナーリードA)
8絶縁フィルム
リード支持板19
4リード
(インナーリードB)
5LSIチップ
10ラバー
(B)
6LSIパッケージ
7ボンディングパッド
5LSIチップ
10ラバー
3リード(インナーリードA)

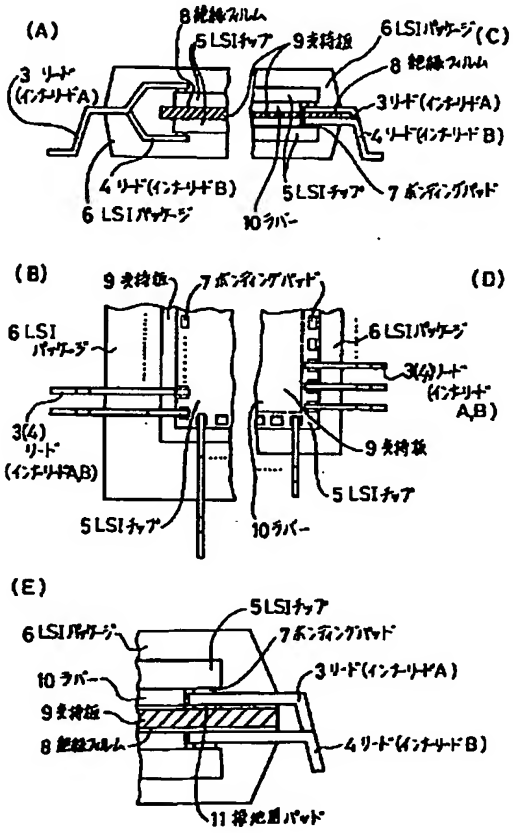
【図3】


(C)
7 ボンディングパッド
9 支持板
5 LSIチップ
リード(インナーリードB)
4
3 リード(インナーリードA)
LSI パッケージ6
8 絶縁フィルム
5 LSI チップ
(D)
4(3)リード(インナーリードA,B)
7 ボンディングパッド
5 LSI チップ
6 LSI パッケージ
リード支持板19
9 支持板
3
リード
(インナーリードA)
4 リード(インナーリードB)

【図4】


(A)
6 LSI パッケージ
9 支持板
7 ボンディングパッド
5 LSI チップ
3 リード(インナーリードA)
8 絶縁フィルム
19 リード支持板
4 リード(インナーリードB)
5 LSIチップ
(B)
6 LSI
パッケージ
7 ボンディングパッド
3 リード(インナーリードA)
5 LSIチップ

【図5】


(A)
8 絶縁フィルム
5 LSIチップ
9 支持板
6 LSIパッケージ
(C)
3 リード
(インナーリードA)
8 絶縁フィルム
3 リード(インナーリードA)
4 リード(インナーリードB)
4 リード(インナーリードB)
5 LSIチップ
7 ボンディングパッド
6 LSIパッケージ
10 ラバー
(B)
9 支持板
7 ボンディングパッド
(D)
6 LSI
パッケージ
6 LSIパッケージ
3(4)リード
(インナーリード
A,B)
3(4)
リード
(インナーリードA,B)
9 支持板
5 LSIチップ
5 LSIチップ
10 ラバー
(E)
5 LSIチップ
6 LSIパッケージ
7 ボンディングパッド
10 ラバー
3 リード(インナーリードA)
9 支持板
8 絶縁フィルム
4 リード(インナーリードB)
11 接地用パッド